NXP Semiconductors
Application Notes

Document Number: AN13461
Rev. 0, 11/2021

NXP Microcontroller Troubleshooting Checklist

by: NXP Semiconductors

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1. Introduction

This application note discuss the points that you can use to troubleshoot microcontroller when there is a malfunction.

2. Functional description

The following points needs to be monitored while the NXP microcontroller (uC) is still mounted on a malfunctioning module. These points are considered helpful for diagnosing basic failure modes and are intended to help identify if the failure mode is related to the module or to the uC itself. Note that not all NXP uC's will have all options detailed below due to varying design features and the reference manual for the uC under analysis should be reviewed for confirmation.

1. Voltage Levels: Verify that all uC power supplies measured are within the datasheet voltage specifications. It is fairly important to capture this data using an oscilloscope at time when the faulty behavior is observed. The stability of the power supply could be masked by a digital multimeter as this tool averages data.

2. Current Consumption: During the failing

condition(s), the current consumption to the module or better yet to the power rails of the uC can be measured using an ammeter or current probe that can be monitored with an oscilloscope. In this approach, one can easily determine if the failure is associated with large changes in current that could indicate that a power supply may be momentarily driven out of specification. If a uC is in a Stay in Reset (SiR) condition, it could be due to repeated failed attempts to execute a Built In Self Test (BIST). During BIST execution, a large current draw may be seen during a particular partition. If the input voltage is not maintained during the current spike, the voltage may dip and cause a reset. The BIST would again execute assuming the voltage raises but would again see the large current spike and another reset would occur. This information provides a deeper understanding of what could be causing a SiR condition. The following figure shows an example current profile of a successful M/LBIST execution.

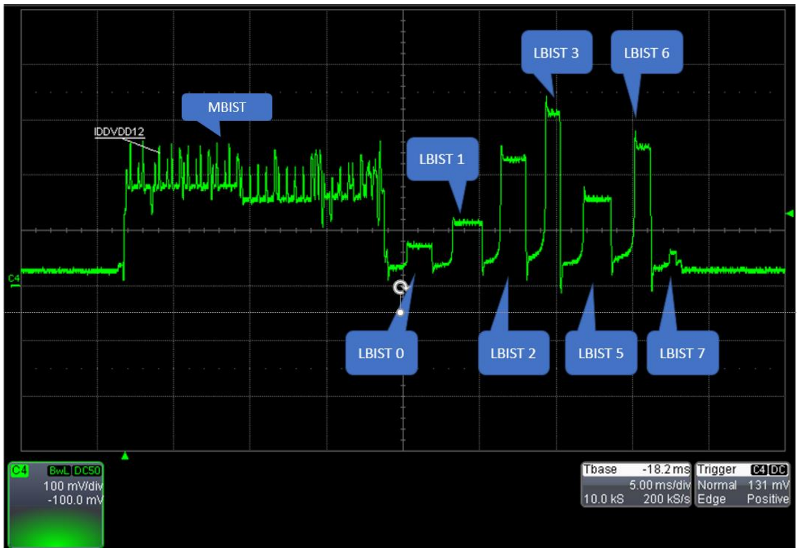

Figure 1. **Successful M/L BIST execution profile**

3. External Clock Source(s): If there is an external clock source attached to the uC i.e crystal. It is important to check whether or not the clock source is oscillating at the expected frequency may provide insight as to where in application code or reset sequence failure is occurring. Note that the output side of the uC ie. XTAL to the crystal should be probed, to check load to the crystal with an oscilloscope probe.
4. Reset Lines (part1): The reset line(s) of the micro can be monitored to determine if the uC is out of reset or not. There are typically two resets, POR_B (input to uC) and RESET_B (bidirectional). There can be a lot of reasons why the uC is unable to assert the RESET_B from internal sources.
    a. Power supply voltages are the typical reason why a uC would assert the RESET_B pin via a Low Voltage Detect (LVD) circuit or similar. Disconnecting the RESET_B pin of the micro from the module will determine if the source of the reset assertion is due to an internal vs external source.
    b. If JTAG is available, typically there is a register within the uC that can identify the reset source ie. SIU.RSR or RGM_FES/DES.

5. Reset Lines (part2): The behavior of these reset lines should be closely monitored with an oscilloscope during the time span of the failure observation. Reset duration and the amount of reset assertions can provide valuable data points and help to differentiate between a deterministic Software Watchdog Timer (SWT) reset for example or multiple resets in a row which would be indicative of a potential reset escalation or an unstable power supply. The following figure shows an example of a period reset resulting from a reset escalation that ultimately leads to a SiR condition.

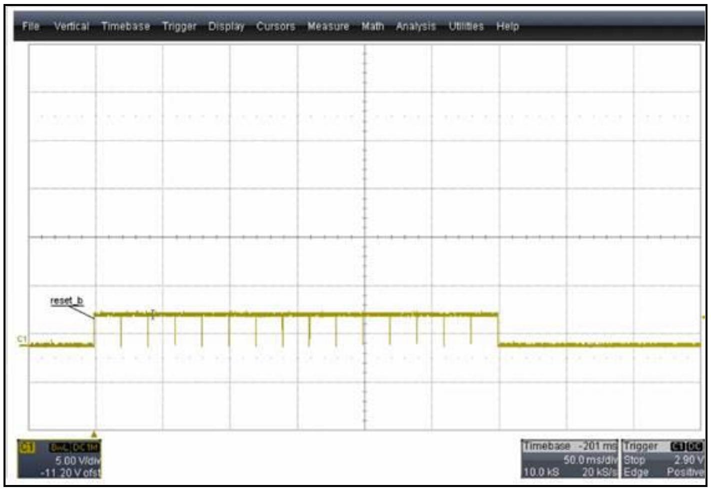

Figure 2. **Reset escalation**

6. FCCU: If the uC contains a Fault Collection and Control Unit (FCCU), the pins associated with the FCCU can be monitored to identify abnormal behavior. Additionally, if debugger access is available, the FCCU can be read to determine fault source.
7. Memory Initialization: Microcontrollers/Microprocessors may contain SRAM or system RAM. But there are also module internal RAMs (like the DMA's service descriptors, FlexCAN message buffers, etc.). All of these SRAMs/RAMS must be initialized prior to their utilization. At the time when the error shows up it should be validated that all these memories are properly initialized.
8. Error Reporting Modules: If the uC contains an ECSM or ERM module, the error syndrome information provided by/in this module can be read and incorporated in the analysis to help identify improperly programmed flash content containing ECC errors.
9. Code/Data Consistency: Whether the code that the uC is executing resides in embedded memory or external, the data should be checked for consistency. Expected data and/or the data could be reprogrammed into another known good module with a known good uC to corelate the behavior (only if security features allow this).
10. MBIST/LBIST: If the uC contains Logic and/or Memory Built In Self Test (L/MBIST), execution results may provide valuable information regarding failure diagnosis. The benefits of executing BIST on a module is that if a failure is identified there, when the uC is placed on an EVB or ATE, the same BIST can be rerun under same conditions offering an excellent correlation environment.
11. JTAG Check: Successfully reading a valid JTAG ID is a simple check that informs that all basic power is being provided at adequate levels. This is possible if the micro is in a Stay in Reset

(SiR) condition. If the uC is in a SiR condition due to a Power On Reset (POR) assertion or a reset source that prevents the uC from exiting Reset Phase 1 of the reset sequence, JTAG communications will not be available.

12. Alternative Boot Modes: If the uC has various boot modes configurable via pin states during reset, exercising alternate boot modes may identify if the failure is related to only one boot mode or all boot modes.
13. Standby (and power mode) Relation: If the module supports multiple power modes such as Run or Standby mode, it may be valuable information to assess whether the faulty behavior is related to one of these specific modes.
14. Injection Current: Check whether there are situations in which current injection exceeds the electrical specification of the uC. This may show up as an Analog to Digital Converter (ADC) failing measurement
15. Temperature/Power Impact to Intermittent Failure Modes: Check whether the reproducibility of the issue can be influenced by temperature or marginal variation of the power supply levels if possible. Varying temperature or voltage conditions could help to identify possible mechanical connection issues with the uC. Furthermore, applying slight downward pressure to the top of the uC could also help in this respect.
16. Temporal/Chronological Differences: Compare the faulty device's temporal/chronological behavior with a known good component. Example:
    - A good component asserts GPO[14] to 1 after 25ms and the uC sends the first CAN message after 50ms.
    - A bad component asserts GPO[14] to 1after 40ms and the uC sends the first CAN message after 200ms.
17. Correlation with Reference Module: (This is not the same as an A-B-A Swap) Regardless of the failure mode, having a reference module/uC on hand to compare observations provides a good sanity check for the analyst. This will help answer questions such as "Is what I am seeing expected or not and if not, how exactly does it differ?"
18. A-B-A Swap: As a last confirmation of failure, it is recommended perform an A-B-A swap to identify if the failure follows the module or the uC. When performing this sequence, the suspect uC is placed on a known good module and a known good uC is placed on the suspect module. If the failure follows the suspected uC, it should be returned to NXP for analysis.

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Document Number: AN13461
Rev. 0
11/2021